NBS TECHNICAL NOTE 958

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Four Versatile MIDAS Compatible Modules

NATIONAL BUREAU OF STANDARDS

The National Bureau of Standards[1] was established by an act of Congress March 3, 1901. The Bureau's overall goal is to strengthen and advance the Nation's science and technology and facilitate their effective application for public benefit. To this end, the Bureau conducts research and provides: (1) a basis for the Nation's physical measurement system, (2) scientific and technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to promote public safety. The Bureau consists of the Institute for Basic Standards, the Institute for Materials Research, the Institute for Applied Technology, the Institute for Computer Sciences and Technology, the Office for Information Programs, and the Office of Experimental Technology Incentives Program.

THE INSTITUTE FOR BASIC STANDARDS provides the central basis within the United States of a complete and consistent system of physical measurement; coordinates that system with measurement systems of other nations; and furnishes essential services leading to accurate and uniform physical measurements throughout the Nation's scientific community, industry, and commerce. The Institute consists of the Office of Measurement Services, and the following center and divisions:

Applied Mathematics — Electricity — Mechanics — Heat — Optical Physics — Center for Radiation Research — Laboratory Astrophysics[2] — Cryogenics[2] — Electromagnetics[2] — Time and Frequency[2].

THE INSTITUTE FOR MATERIALS RESEARCH conducts materials research leading to improved methods of measurement, standards, and data on the properties of well-characterized materials needed by industry, commerce, educational institutions, and Government; provides advisory and research services to other Government agencies; and develops, produces, and distributes standard reference materials. The Institute consists of the Office of Standard Reference Materials, the Office of Air and Water Measurement, and the following divisions:

Analytical Chemistry — Polymers — Metallurgy — Inorganic Materials — Reactor Radiation — Physical Chemistry.

THE INSTITUTE FOR APPLIED TECHNOLOGY provides technical services developing and promoting the use of available technology; cooperates with public and private organizations in developing technological standards, codes, and test methods; and provides technical advice services, and information to Government agencies and the public. The Institute consists of the following divisions and centers:

Standards Application and Analysis — Electronic Technology — Center for Consumer Product Technology: Product Systems Analysis; Product Engineering — Center for Building Technology: Structures, Materials, and Safety; Building Environment; Technical Evaluation and Application — Center for Fire Research: Fire Science; Fire Safety Engineering.

THE INSTITUTE FOR COMPUTER SCIENCES AND TECHNOLOGY conducts research and provides technical services designed to aid Government agencies in improving cost effectiveness in the conduct of their programs through the selection, acquisition, and effective utilization of automatic data processing equipment: and serves as the principal focus wthin the executive branch for the development of Federal standards for automatic data processing equipment, techniques, and computer languages. The Institute consist of the following divisions:

Computer Services — Systems and Software — Computer Systems Engineering — Information Technology.

THE OFFICE OF EXPERIMENTAL TECHNOLOGY INCENTIVES PROGRAM seeks to affect public policy and process to facilitate technological change in the private sector by examining and experimenting with Government policies and practices in order to identify and remove Government-related barriers and to correct inherent market imperfections that impede the innovation process.

THE OFFICE FOR INFORMATION PROGRAMS promotes optimum dissemination and accessibility of scientific information generated within NBS; promotes the development of the National Standard Reference Data System and a system of information analysis centers dealing with the broader aspects of the National Measurement System; provides appropriate services to ensure that the NBS staff has optimum accessibility to the scientific information of the world. The Office consists of the following organizational units:

Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Standards — Office of International Relations.

---

[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.

[2] Located at Boulder, Colorado 80302.

Four Versatile MIDAS Compatible Modules

Michael A. Lind and Joel B. Fowler

Institute for Basic Standards
National Bureau of Standards
Washington, D.C. 20234

U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, Secretary

Dr. Sidney Harman, Under Secretary
Jordan J. Baruch, Assistant Secretary for Science and Technology

NATIONAL BUREAU OF STANDARDS, Ernest Ambler, Acting Director

Issued November 1977

National Bureau of Standards Technical Note 958
Nat. Bur. Stand. (U.S.), Tech. Note 958, 34 pages (Nov. 1977)
CODEN: NBTNAE

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1977

For sale by the Superintendent of Documents, U.S. Government Printing Office
Washington, D.C. 20402 - Price $1.40

Stock No. 003-003-01866-0

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

PAGE

NOTE

Certain commercial products are identified in this paper in order to specify adequately the experimental procedure, or to cite relevant examples. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the products or equipment identified are necessarily the best available for the purpose.

FOUR VERSATILE MIDAS COMPATIBLE MODULES

Michael A. Lind* and Joel B. Fowler
Radiometric Physics Section
Optical Physics Division
Institute for Basic Standards

Four versatile MIDAS compatible modules are documented. These modules include a precision digital to analog converter, a programmable up/down counter, a high speed stepping motor indexer, and an amplifier controller-filter-V/F converter.

Key Words: Data acquisition system; MIDAS; MIDAS amplifier controller; MIDAS digital to analog converter; MIDAS modules; MIDAS stepping motor indexer; MIDAS up/down counter.

INTRODUCTION

The MIDAS (Modular Interactive Data Acquisition System) is widely used at the National Bureau of Standards as a versatile interface between experimental apparatus and a computer. A general description of the MIDAS is available in NBS Technical Note 790. Although many modules for this system are now commercially available, not all experimental situations can be adequately controlled by the existing designs.

The purpose of this Technical Note is to document four modules that have been developed in the Electro-Optics Group at the National Bureau of Standards for use in their computer controlled experiments. The versatility of these four modules make them suitable for use in a wide variety of experimental situations that cannot be handled by the existing commercial modules.

The four modules described in this publication are: (1) a high precision digital to analog converter (DAC), (2) a fully programmable up/down counter with a compare register and precision time base, (3) a high speed stepping motor indexer with fully adjustable output parameters, and (4) an amplifier controller that controls a Keithley Model 18000 programmable current amplifier and has an on-board precision filter and voltage to frequency converter for long-term signal averaging.

---

*Present address: Battelle Northwest, P. O. Box 999, Richland, CA 99352.

PRECISION DAC

MODULE DESCRIPTION

The precision DAC module converts a four digit input from the MIDAS bus into an analog level. An input of ØØØØ presents a voltage of 0.00000 ±.00004 volts at the output (when properly adjusted for zero offset). An input of 9999 presents 9.9990 ±.0005 volts at the output. The output is linear to ±.3 mV and has a maximum worst case drift error of .5mV. Each BCD count is equivalent to 1 mV and settling time is 50 μsec.

PRE-OPERATION ADJUSTMENTS

Current output or voltage output may be selected (see Fig. 1) via the strapping option on the board: I = I_{out}, V = V_{out}, O = Output pin (I_{out} should never be hooked to V_{out} or converter will be destroyed).

The offset should be adjusted as follows: select module, reset module, then adjust the offset pot (R7) for 0.0000 volts at the analog output.

Next input 9999 to module (i.e. 9999:) and adjust gain pot (R9) for 9999 mV at the analog out (or -1.24987 mA in current mode).

Recheck the offset adjustment as discussed above, if necessary readjust R7. If this adjustment is changed it will be necessary to recheck the gain adjustment also.

MIDAS COMMANDS

#	puts MIDAS into command mode
B-M	selects module position on bus
;	reset DAC logic (not necessary except to zero output)
0-9	input number of up to four digits to be converted
:	load and go

EXAMPLE: #H1234: changes the output from its previous value to 1234 mV.

CIRCUIT DESCRIPTION

A complete circuit diagram of DAC module is shown in Fig. 1. The board layout and parts list is shown in Fig. 2.

Chip U4 decodes the presence of "0-9", ":" and ";" from the MIDAS bus. The occurrence of an integer from 0 to 9 shifts the BCD data from the command bus lines ($\overline{C1}$, $\overline{C2}$, $\overline{C3}$ and $\overline{C4}$) into shift registers U9, U10,

U11 and U12 respectively. When a ":" is decoded, a "GO" (output of A4 pin 4) is created whose leading edge strobes the contents of U9, U10, U11 and U12 into latches U16, U17, U18 and U19 respectively. The trailing edge of "GO" then triggers the monostable U7, the $\overline{Q}$ output of which resets the shift registers to Ø. The output of the latches then drives the digital to analog converter chip (U18). The logic is reset by either a decoded ";" from the data bus or an "init" from the MIDAS controller.

The output of the DAC ranges from 0 to -1.24987 mA. This current is converted to a voltage output by an amplifier (U19) utilizing the internal feedback resistor in the DAC to obtain the output of 0 to 9.999 volts. The gain and offset of the DAC are adjustable by potentiometers R9 and R6 respectively. The ±15 VDC supply for the DAC is obtained from a voltage to voltage switching converter (U17) operating at approximately 40 kHz.

More information on the DAC chip may be obtained from Publication PDS-332 available from Burr-Brown Research Corporation.

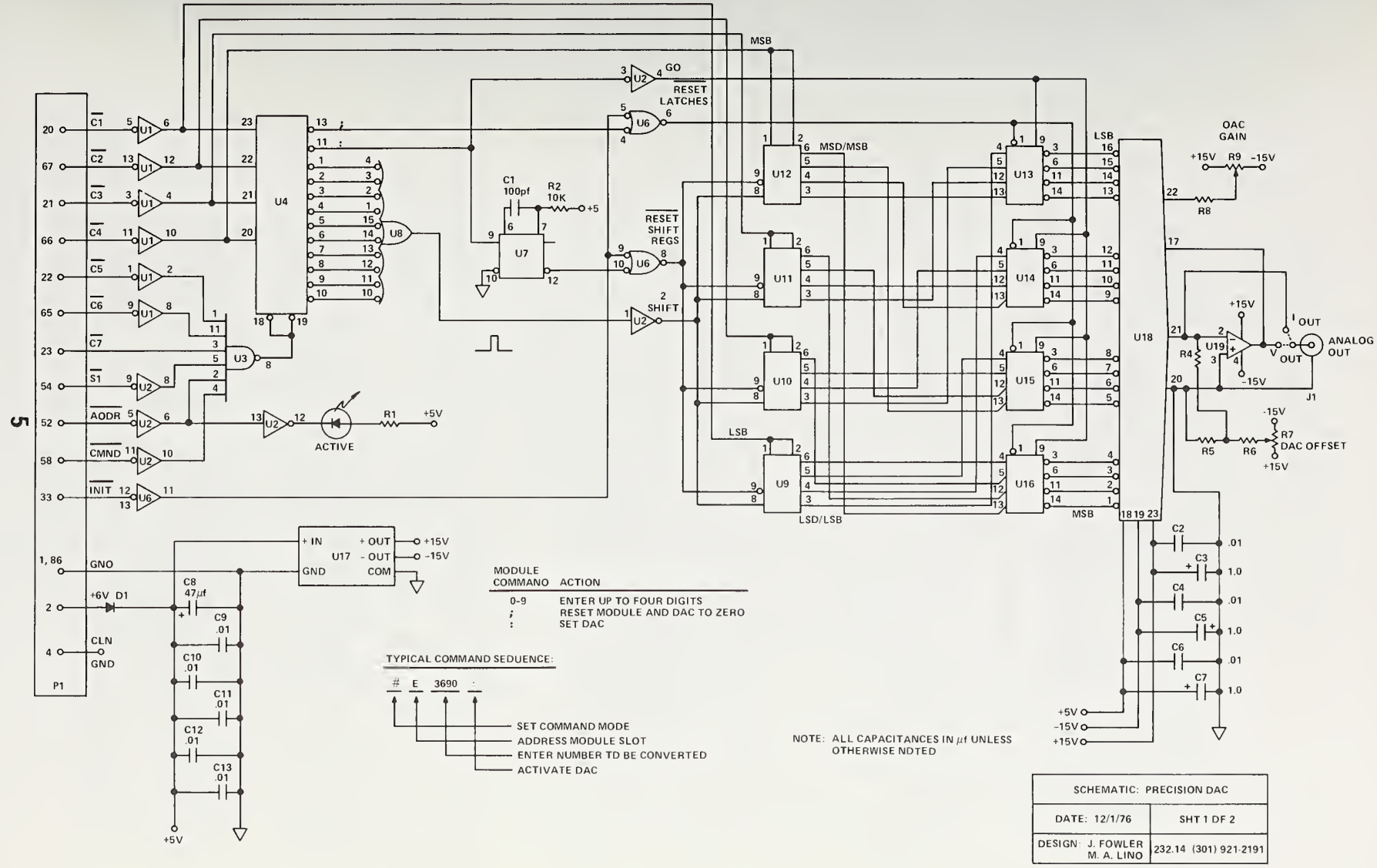
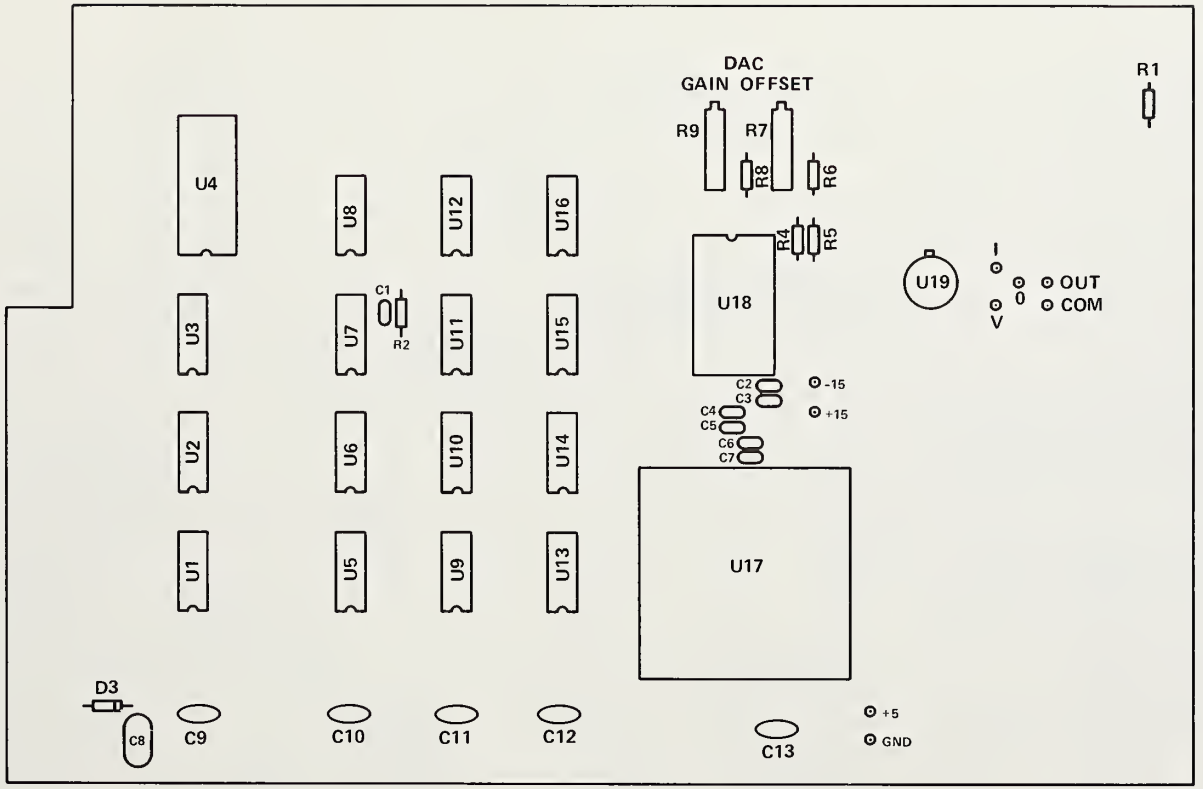


Fig. 1: Schematic diagram for precision DAC.



ACTIVE COMPONENTS:

U 1	7404
U 2	7404
U 3	7430
U 4	74154
U 5	—
U 6	7408
U 7	74123
U 8	74133
U 9	74164
U10	74164
U11	74164
U12	74164
U13	74175
U14	74175
U15	74175
U16	74175
U17	DATEL BPM-15/100-D5
U18	DAC70-CCD-I BURR-BROWN

D1	1N4001

PASSIVE COMPONENTS:

R1	470Ω
R2	10K
R3	—
R4, R6	150K
R5	6.2K
R7	10K 15 TURN W/W
R8	510K
R9	50K 15 TURN W/W
C1	100pf SILVER MICA
C2, C4, C6, C9–C13	.01μf CERAMIC
C3, C5, C6	1μf TANT
C8	100μf TANT

LAYOUT: PRECISION DAC	
DATE: 12/1/76	SHT 2 OF 2
DESIGN: J. FOWLER M. A. LIND	232.14 (301) 921-2191

Fig. 2: Layout and parts list for precision DAC

PROGRAMMABLE UP/DOWN COUNTER

MODULE DESCRIPTION

This versatile MIDAS module features a presetable and readable UP/DOWN counter, a presetable compare register, and a programmable time base. It can be applied to a wide variety of experimental situations such as normal event counting, quadrature up/down counting of optical and magnetic encoders, long term integration of polarity sensitive voltage controlled oscillator (VCO) frequency measurements, or as a self-contained fully programmable time base.

OPERATION

All front panel connections are TTL compatible. A low or logic "0" input may be generated by a closure to ground. The schmidt trigger inputs generally provide sufficient hysteresis to allow operation at high or logic "1" levels with no pull-up resistor. In extremely noisy environments a 1 kΩ pull-up resistor is recommended.

Input

The counter changes on the positive transition of the COUNTER IN input. It will increment when the UP/DOWN input is high and decrement when the UP/DOWN input is low. The maximum counting rate is limited to 1 MHz and the UP/DOWN input may be changed .75 μs prior to the positive transition of the count input. The counter counts through zero and automatically keeps track of the sign (i.e., when counting down the counter will display 2, 1, 0, -1, -2, etc.). Resetting or presetting the counter always forces the sign positive, thus only positive numbers may be loaded into the counter and the compare register.

Output

There are three basic outputs from the counter which can be directed to the COUNTER OUT connector via the switches at U17 (see Fig. 3). These signals appear as follows:

zero: If #6 is closed the output will go high for one count period on the positive edge of the count input when all decades of the counter contain zero. This function is inhibited during a load counter operation.

equal: If #4 is closed the output will go high for one period when the contents of the counter and compare registers are equal. This function is also inhibited during a load counter or load register operation.

carry: If #2 is closed the output will go high with the leading edge of the count impulse at the count of

000000 when counting up or at 999999 when counting down, and it goes low with the negative going edge of the same count pulse. This "carry" signal may be used to cascade counter modules if more than six decades are needed.

There is some delay in processing these signals. Therefore the counting frequencies should be limited to 500 kHz if they are to be used.

The counter may be gated in one of three ways:

1. Internally via direct commands from the MIDAS.

2. Internally via the programmable time base discussed below.

3. Externally via the EXT GATE IN. A low signal inhibits the counter if the MIDAS controlled gate is closed and the time base gate is not active.

These three gating modes are "OR" ed together so that the counter is enabled if any one of these gates are active.

The gating signal is available at the GATE OUT terminal for external use. This output will be low true when the gate is open and the counter is enabled. By using the GATE OUT signal more than one module may be controlled from the same time base.

The module will signal the controller that it is busy when the gate is activated by any one of the three methods mentioned above. The busy signal to the controller will be terminated, a module done signal generated (a wait will be satisfied) and the counter will be inhibited when one of the following conditions are satisfied:

1. The gate is closed by one of the methods mentioned above.

2. Switch #5 is closed and a zero count is detected on the counter.

3. Switch #3 is closed and the contents of the counter and the compare register are equal.

4. Switch #1 is closed and a carry is generated by the counter.

The time base oscillator output is available at the TIME BASE OUT connector. This signal is present at all times and is periodic with a period that is determined by the programmed time base. For the highest accuracy it is suggested that all applications requiring the use of the time base be synchronized with the falling edge of this signal. The output will make a negative transition within 500 ns of a "T" command regardless of its previous state. The overall accuracy of the time base is limited to approximately one part in 10^5.

MIDAS COUNTER AND REGISTER COMMANDS

P	select counter to be loaded
Q	select compare register to be loaded
R	reset counter and close gates
>	ready counter or register for input
0-9	up to six digits may be loaded into the counter or register
<	load the number into the counter or register
U	dump the contents of the counter onto the MIDAS bus
[	open counter gate
]	close counter gate

The P and Q commands control a flip-flop, therefore, if the counter only is to be loaded, the P command need be given only once after the module has been powered up.

It should be noted that there is no direct way to clear the compare register, only reloading it will change its contents.

As mentioned above the counter counts through zero and keeps track of the sign automatically. Because all the counter circuitry is enclosed in one LSI chip, one problem does arise which will give an incorrect count and sign. If the counter is reset to zero and one starts to count down, after the first count the device will read +999999, then 999998 etc. This problem can be circumvented by presetting the counter to 1 before gating. The count will then read 1, 0, -1, -2, etc. No problem exists if the first count is positive.

MIDAS TIME BASE COMMANDS

Programming the time base requires a three character sequence:

S	selects the time base to be programmed
0->	selects period of time base
T	triggers the time base by resetting it to max and enabling the time base gate to the counter

COMMAND	GATE OUT TIME	TIME BASE OUT
0	1 µsec	1 MHz
1	10	100 kHz
2	100	10
3	1 msec	1
4	10	100 Hz
5	100	10
6	1 sec	1
7	10	.1
8	100	.01
9	1 min	
:	1 hr	
;	10 min	
<	0	
=	0	
>	20 msec	

PROGRAMMING EXAMPLES

The command sequence

#HRP>1234<

puts the MIDAS in command mode, selects the bin position H containing the counter module, resets the counter, and loads the number 1234 into the counter. This number will be visible on the front panel display.

Q>56789<

loads the number 56789 into the register.

S6T

triggers the time base gate open for 1 second.

S6RT*

opens the counter gate for one second while the MIDAS is in a WAIT mode. After one second the wait is cleared and the MIDAS continues.

The time base and the counter can be combined to provide a high accuracy fully programmable time delay. To do this set switch 3 to ON, and 5 and 6 to OFF. Connect TIME BASE OUT to COUNTER IN. The command sequence

#H]Q>500<S4R[*

selects the module, closes the gate, loads 500 into the compare registers, sets the time base to 100 Hz, resets the counter, opens the gate, and puts the MIDAS in WAIT mode. The elapsed time in 1/100 second intervals is displayed on the front panel. The WAIT clears after five seconds and the MIDAS continues.

CIRCUIT DESCRIPTION

A complete set of schematic diagrams for this module is shown in Fig. 3 and 4 . The printed circuit board layout and parts list is illustrated in Fig. 6.

The major portion of this module is designed around a MOSTEK MK 50395N MOS counter chip (U53). This chip contains a six digit BCD counter, a six digit static register, a digital comparator, a latch, a scan counter, a multiplexer and decoder driver. A complete description of the chip is available from MOSTEK in their application notes and data sheets.

Because all interaction with the chip must be done synchronously with its scan clock, a buffer between the MIDAS bus and the chip is necessary. This four bit by six digit buffer (U41-U44) is used both to load the counter from the command bus and to unload the counter onto the data bus of the MIDAS. A complete set of timing diagrams for the loading and unloading sequence that are described below is shown in Fig. 5.

The control signals for this module are decoded from the ASCII characters on the command bus lines $\overline{C1}$-$\overline{C7}$ via U8, U11, U12, U19 and U16 and are strobed by a combination of S1, CMND and ADDR. The following sequence of events loads a number into the counter or compare register. A "P" input from the bus will set flip-flop U26B and a "Q" will reset the same flip-flop, selecting either the counter or compare register. A ">" will then clear the buffer and set flip-flop U23A steering the buffer registers (U41, U42, U43 and U44) to the command bus data lines ($\overline{C1}$, $\overline{C2}$, $\overline{C3}$, and $\overline{C4}$) via multiplexer U45. Any digit "0-9" input on the command bus will produce the strobe NUMBER and shift the number present on the bus into the buffer. When the desired digits have been input, a "<" resets U23A which steers the multiplexer (U45) back to the counter output lines. It also sets U33A and resets U33B. This synchronizes the load sequence of the counter chip with the proper digit strobes from the counter chip.

The data input to the counter chip (U53) must be multiplexed using the digit strobes supplied by the chip. The leading edge of the next strobe for digit one (U28 pin 12) clocks the Q output of U33A high and the $\overline{Q}$ output of U33B low. This in turn sets U26A which enables the proper load line to U53 (counter or compare register). On the trailing edge of this first digit strobe the buffer register shifts the first digit to pin 9 of U41, U42, U43 and U44. On the leading edge of the next digit strobe this data is loaded into U53, and on the trailing edge, the shift registers are clocked again. This continues until the sixth digit is loaded by the re-occurrence of the digit 1 strobe. On the trailing edge of the second digit 1 strobe, U26A is clocked low which disables the load lines to U53 thus ending the load cycle.

The "U" initiates the sequence that dumps the contents of the counter onto the MIDAS data bus. The "U" strobe resets the counter U39 to "9" and sets flip-flop U32A. The Q output of U32A enables the D input of U32B. On the trailing edge of digit strobe 1, the Q output of U32B is clocked high, enabling the buffer register clock. Anomalies within the digit strobe timing on the counter chip cause the BCD data at the counter output to remain valid for at least 100 ns after the leading edge of the next digit strobe. Thus, the leading edge of digit strobe 2 is a convenient time to clock the data from digit 1 into the buffer register. The remaining five digits are shifted into the buffer on the leading edges of digit strobes 3, 4, 5, 6 and 1 respectively.

On the trailing edge of the second occurrence of digit strobe 1, U32B is clocked low, disabling the clocks to the buffer. When the $\overline{Q}$ output of U32B goes high, U34B is clocked high starting the dump cycle to the MIDAS data bus. At this point all three inputs to U30A are high which triggers the monostable U35A. The trailing edge of the pulse output by U35A triggers the monostable U40A. Plus or minus from U23B is encoded by portions of U2 and strobed onto the data bus by the first DATAS. The buffer register (U41-U44) is shifted one place on the trailing edge of the pulse from U40A and state counter U39 is clocked which rolls it over from "9" to "0" thus disabling the plus or minus gating and enabling the outputs from the buffer to the bus.

Just after the leading edge of DATAS, the controller forces CONTB (U30A pin 3) low until the data has been taken from the bus. When CONTB goes high again U35A is triggered once again starting another output cycle. This cycle is identical to the last cycle except that the data from the buffer (in this case, the MSD of the counter output) is strobed onto the bus. This sequence continues until all six output digits are strobed onto the data bus. After the seventh data strobe, the state counter contains the number "6" (9, 0, 1, 2, 3, 4, 5, 6). The "6" is decoded by U38C whose output disables any further data strobes, forces an MEOT onto the MIDAS bus and resets U34B ending the unload sequence.

The counter chip (U53) has a self-scanning, multiplexed display output consisting of six digit strobes and seven segment outputs which drive an LED display.

The front panel inputs to the counter chip (UP/DN, COUNT INPUT and EXT GATE IN) drive schmidt triggers (U25). The COUNT input goes directly to the CNT input of the counter chip. The UP/DN indirectly drives the UP/DN input of the counter chip via U23B and U24C which form a control network to keep the counter from "rolling over" if it counts down thru zero.

The EXTERNAL GATE IN is one of three gate signals at U20 which may disable the CNT INH line to the counter chip, thus permitting counting. Another input is controlled by the output of U13B which enables counting upon receipt of a "[" from the command decoder and disables upon receipt of a "]". The third input is the output of U14A which synchronizes on the on-board time base. These gating functions are also available to the GATE OUT connector.

The counter may be set up via the PC switch (U17) to automatically stop the count on any one or all of the three condition outputs of the counter chip (Ø, =, carry) independent of the gate function mentioned above. These three conditions may also be utilized via "counter out" to gate other counters or devices in the outside world (these are also set up by the p.c. switch).

The on-board time base consists of a 10.000 MHz crystal oscillator which is divided down to 1 MHz by decade counter U58. This square wave drives the LSI time base generator U59. The time base generator U59 divides the 1 MHz input by various integral amounts controlled by the output of latch U60. The latch is loaded whenever a number is decoded from the MIDAS bus preceded by an "S". The output of the time base (pin 1 of U59) is connected to the TIME BASE OUT connector at the front panel.

The counter may be gated by the time base when a "T" is decoded from the control bus. This signal triggers monostable U10A whose output sets U14B and forces the output of U59 to a high state for the period of the monostable. On the following clock pulse from U58, the output of U59 goes low clocking the $\overline{Q}$ of U14A low. This signal disables the counter chip "CNT INH" input and clocks the Q output of U14B low. The "CNT INH" remains disabled for one cycle of the output of U59 when the $\overline{Q}$ output of U14A is clocked high enabling it again.

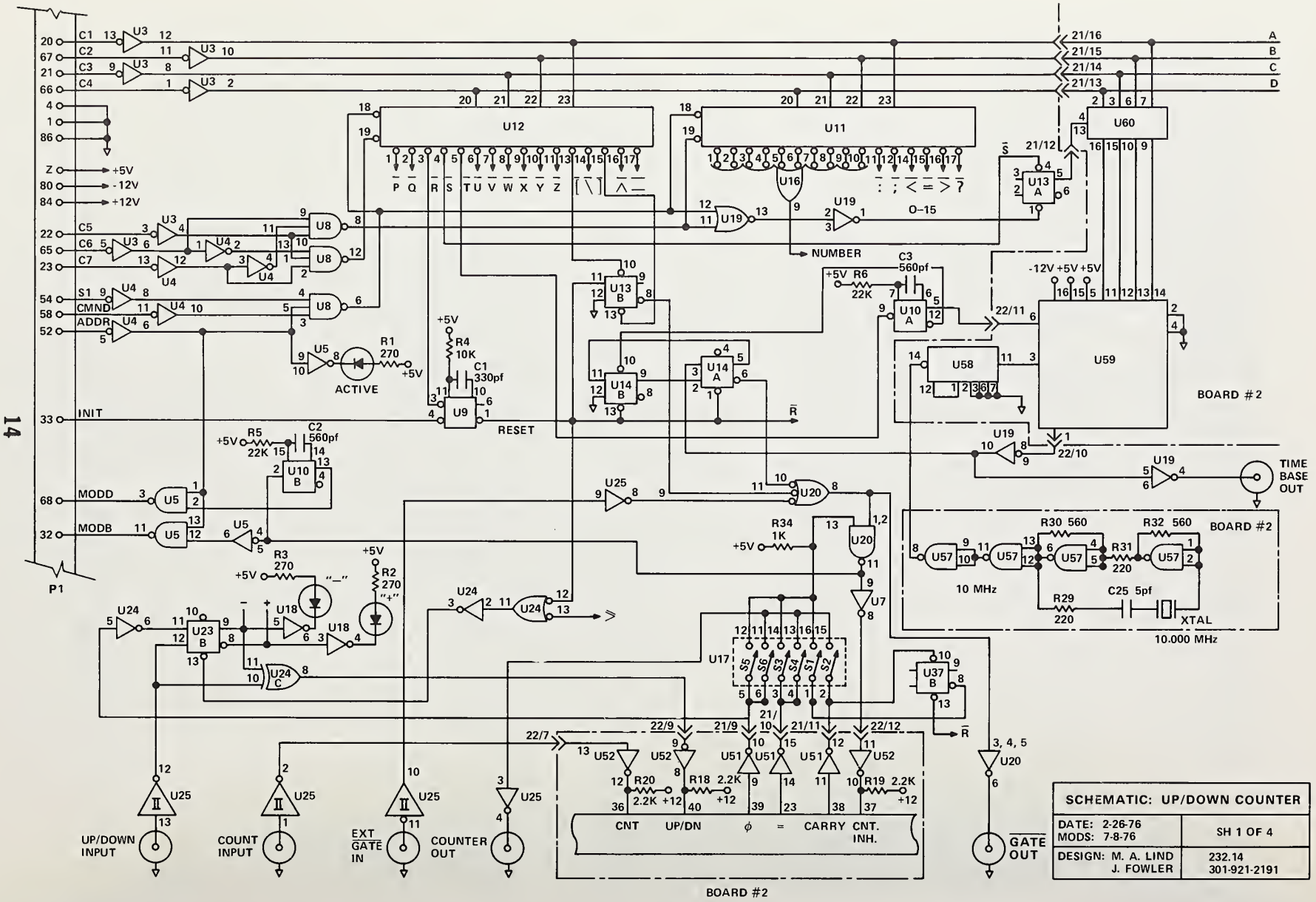


Fig. 3: Schematic diagram for up/down counter: Sheet 1

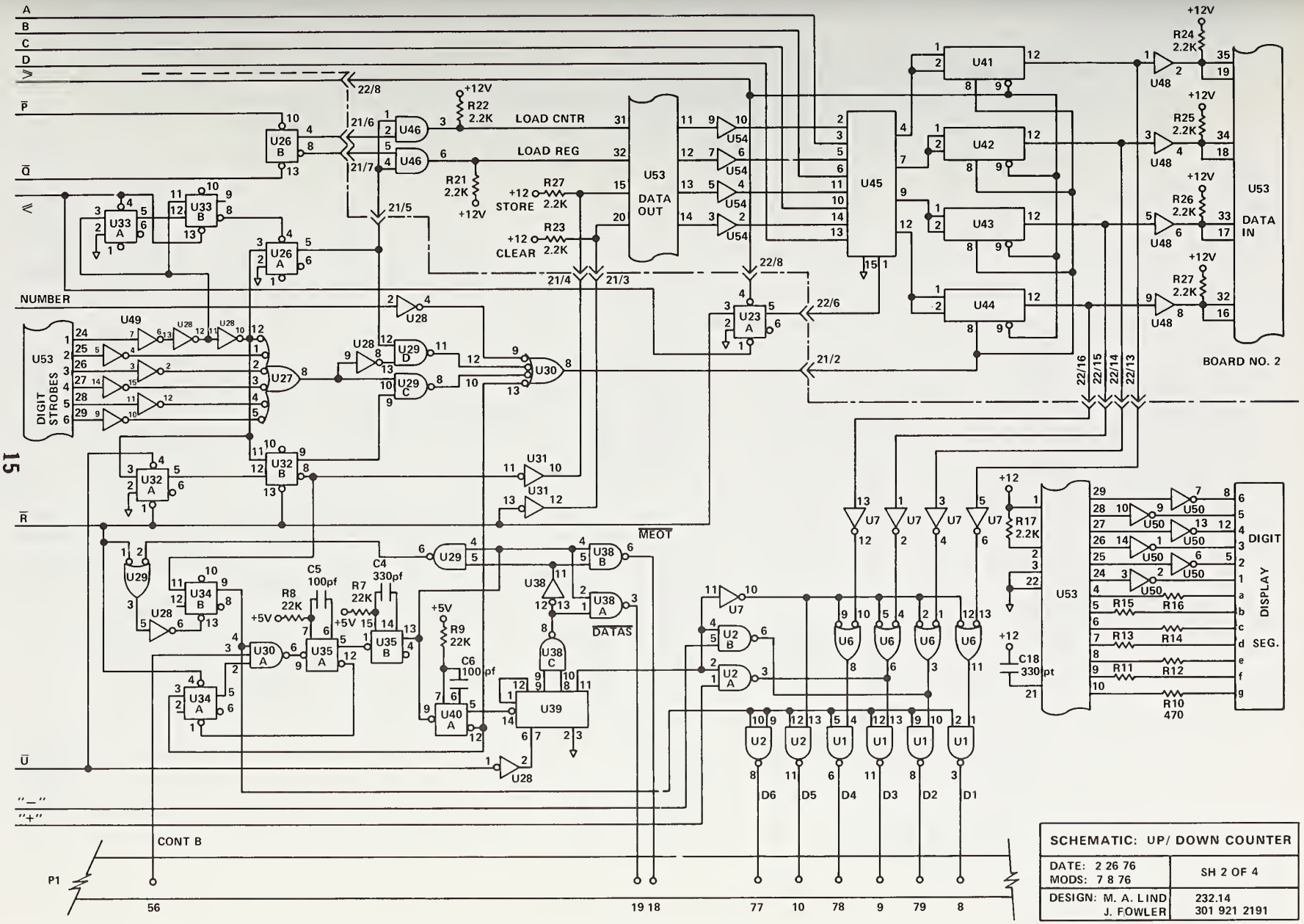
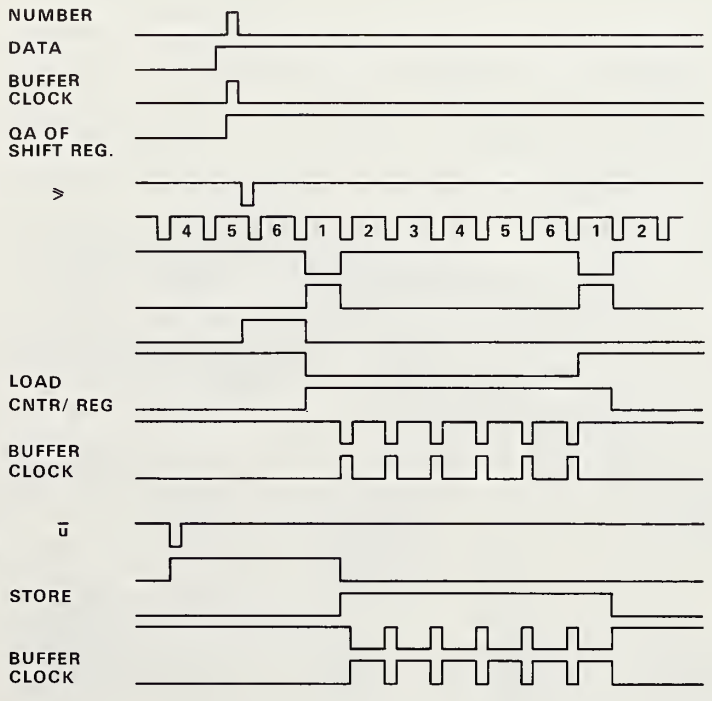


Fig. 4: Schematic diagram for up/down counter: Sheet 2



U16/9	LOAD BUFFER FROM MIDAS BUSS	
U3/12		
U30/8		
U41/3		
U11/16	LOAD COUNTER OR REGISTER FROM BUFFER	
U27/8		
U28/10		
U28/1		
U33/5		
U33/8		
U26/5		
U29/11		
U30/8		
U12/6	LOAD BUFFER FROM COUNTER	
U32/5		
U32/9		
U29/8		
U30/8		

MODULE COMMAND	FUNCTION
>	CLEARS BUFFER AND ENABLES INPUT FROM MIDAS BUSS TO BUFFER
0-9	GENERATES NUMBER STROBE AND ENTERS NUMBER INTO BUFFER
<	LOCKS OUT MIDAS BUSS FROM BUFFER AND STARTS LOAD SEQUENCE OF COUNTER/REGISTER
R	CLEARS COUNTER, RESETS MODULE
U	STARTS UNLOAD SEQUENCE
P	SELECTS COUNTER TO BE LOADED
O	SELECTS REGISTER TO BE LOADED
S	PRESETS TIME BASE LATCH TO ACCEPT NEXT O-? COMMAND
[	OPENS GATE ON COUNTER
]	CLOSES GATE ON COUNTER
T	RESETS TIME BASE TO MAX AND ENABLES TIME BASE GATE

TIME BASE COMMAND	GATE TIME	TIME BASE OUT
0	1 μs	1 MHz
1	10	100 KHz
2	100	10
3	1 ms	1
4	10	100 Hz
5	100	10
6	1 sec	1
7	10	.1
8	100	.01
9	1 MIN	
:	1 HR	
;	10 MIN	
<	0	
=	0	
>	20 ms	

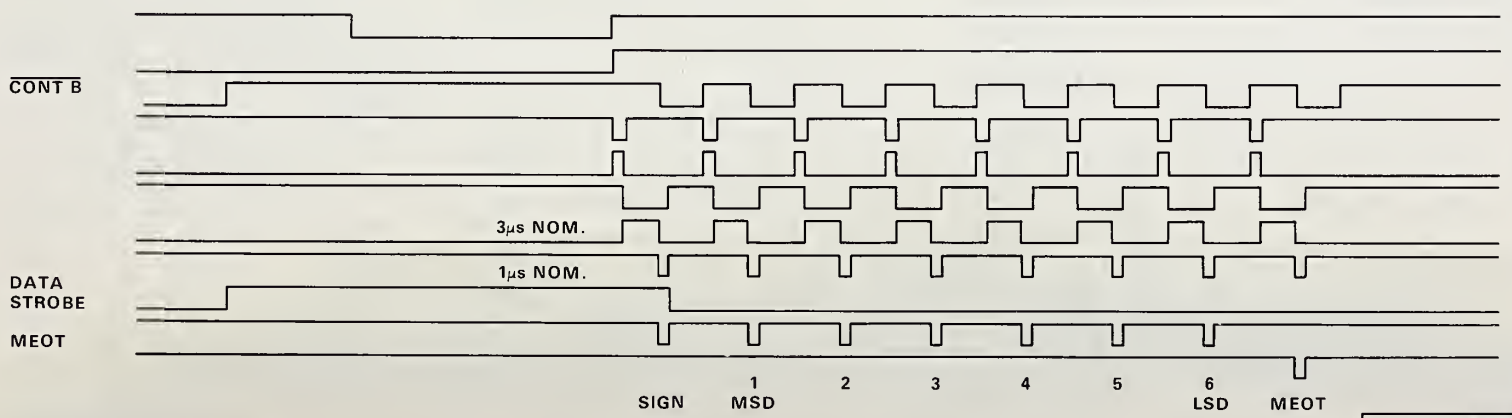
MISC. NOTES:

1) THE TIME BASE IS ALWAYS RESET TO MAX THUS ENABLING THE GATE ON THE NEXT FULL CYCLE OF THE TIME BASE

2) THE COUNTER MAY BE INHIBITED AND THE MODULE BUSY LINE FREED UP IN ANY ONE OF THREE WAYS:
   a) WHEN THE COUNTER COUNTS THROUGH ZERO IF S1 IS CLOSED
   b) WHEN THE COUNTER AND THE REGISTER HAVE EQUAL VALUES IF S3 IS CLOSED
   c) IF THE COUNTER EITHER OVERFLOWS OR UNDERFLOWS IF S5 IS CLOSED
   TWO OR MORE OF THESE FUNCTIONS MAY BE USED SIMULTANEOUSLY IN AN "OR" FASHION

3) THESE THREE FUNCTIONS ARE ALSO AVAILABLE AT THE COUNTER OUTPUT CONNECTOR VIA S2, S4, S6. THE ϕ AND = OUTPUTS ARE MOST USEFUL WHEN USING THE MODULE AS A COUNTING COMPARATOR. THE CARRY ENABLES THE USER TO CASCADE COUNTERS TOGETHER TO OBTAIN MORE THAN 6 DECADES

4) ALL EXTERNAL OUTPUTS AND INPUTS ARE TTL COMPATIBLE



U32/8	DUMP BUFFER ONTO MIDAS BUSS
U34/9	
U30/3	
U30/6	
U35/5	
U34/5	
U35/13	
U40/12	
U39/11	
U38/3	
U38/6	

TIMING DIAGRAMS, UP/ DOWN COUNTER	
DATE: 6/6/76	SH.3 OF 4

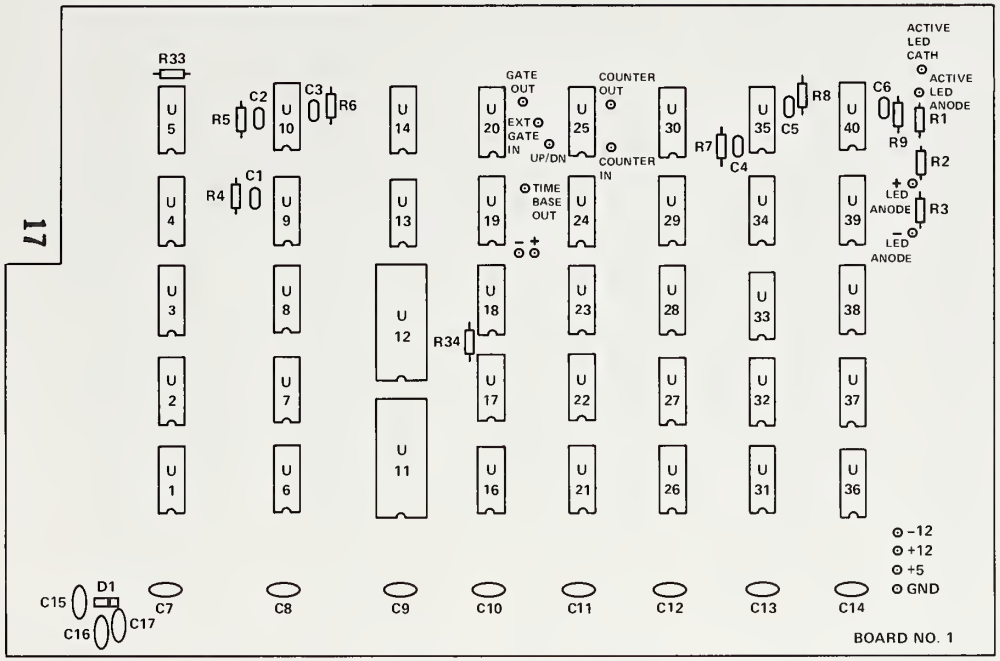
ACTIVE COMPONENTS:

1.	7403	13.	7974	25.	7414 (7406)	37.	7474	49.	4049
2.	7403	14.	7474	26.	7474	38.	7400	50.	75492
3.	7404	15.	——	27.	7430	39.	7490	51.	4049
4.	7404	16.	74133	28.	7404	40.	74123	52.	7406
5.	7403	17.	SWITCH	29.	7400	41.	74164	53.	MK50395
6.	7400	18.	7406	30.	7420	42.	74164	54.	4050
7.	7404	19.	7402	31.	7406	43.	74164	55.	——
8.	7410	20.	7410	32.	7474	44.	74164	56.	——
9.	74121	21.	CONN. A	33.	7474	45.	74157	57.	7400
10.	74123	22.	CONN. B	34.	7474	46.	7409	58.	7490
11.	74154	23.	7474	35.	74123	47.	——	59.	MK5009P
12.	74154	24.	7486	36.	——	48.	7407	60.	7475

D1	1N4001
XTL1	10.000 MHz

PASSIVE COMPONENTS:

R1-R3	270Ω	1/4 W	C1, C4, C18	330pf	SIL. MIC.
R4	10 K	1/4 W	C2, C3	560pf	SIL. MIC.
R5-R9	22 K	1/4 W	C5, C6	100pf	SIL. MIC.
R10-R16	470Ω	1/4 W	C7-C14, C19-C24	.01 or .05 MfD	50V CER. DISKS
R17-R28	2.2 K	1/4 W	C15- C17	100 MfD	20V TANT
R29, R31	220Ω	1/4 W	C25	5pf	SIL. MIC.
R30, R32	560Ω	1/4 W	D1	1N4002 (1N4004)	
R33, R34	1K				



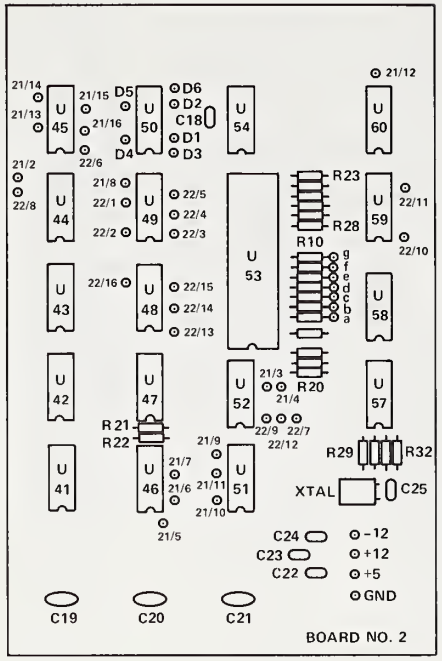


Fig. 6: Layout and parts list for up/down counter.

LAYOUT UP/DOWN COUNTER	
DATE: 7/6/76	SH4 OF 4
DESIGN: J. FOWLER M. A. LIND	232.14 301-921-2191

HIGH SPEED STEPPING MOTOR INDEXER

MODULE DESCRIPTION

This MIDAS compatible module outputs a pulse train for a clock input and a level for directional control suitable for many high speed stepping motor systems. The outputs are directly compatible with the Aerotech System 400 S High Speed Stepping Motor Buffer/Translator or any similar devices using either 12 volt CMOS or 5 volt TTL logic.

The clock rate ramps linearly up and down in frequency to provide for slow starting and stopping speeds and high slew speeds. The minimum and maximum clock rate as well as the ramp slope and pulse width are adjustable to meet the input loading requirements of a specific stepping motor application.

Under program control the module will direct 1-99999 clock pulses to any one of the three output channels. Manual controls are also provided on the front panel to aid in set up and check out of the stepping motor system.

PREOPERATION ADJUSTMENTS

There are several adjustments that should be made before operation with a stepping motor. A scope and a frequency counter will be useful in making these adjustments.

The normal sense of the individual clock outputs may be set at a high or low level by strapping the C1, C2, and C3 terminals between A16 and A21 to the HI or LO post (see Fig. 9). Similarly the maximum voltage of the clock and direction outputs may be strapped to either +5 or +12 at the posts labeled C1, C2, C3, D1, D2, D3 adjacent to 423.

The output pulse width is adjusted using the following procedure. Set the manual controls to CHANNEL 1 and STEP/CONT switch to the CONT position. Attach a scope to the CH1 CLK output and press RUN. Adjust the OUTPUT PULSE ADJUST until the desired pulse width is attained. Further adjustment beyond the range of the pot is possible by replacing the capacitor mounted on the posts adjacent to the pot.

The maximum and minimum frequency may be adjusted in the following way. Monitor test point T2 with a scope or frequency counter. Notice the three terminals adjacent to A36. Short the terminal labeled T1 to LO. Now adjust the MIN FREQ ADJUST pot for the minimum frequency desired. Now short the terminal labeled T1 to HI and adjust the MAX FREQ ADJUST pot for the maximum desired frequency.

The ramp slope may be adjusted using the RAMP SLOPE ADJUST pot. The easiest way to do this is to put a low frequency square wave (0 and 5 volts) on T1 while monitoring the positive side of the capacitor located just above the pot. The ramp slope may be adjusted further by replacing the resistor on the posts near the pot.

Commands: 1-99999 steps to be output

: channel 1 forward

; channel 1 reverse

< channel 2 forward

= channel 2 reverse

> channel 3 forward

? channel 3 reverse

Initializing the module clears everything.

A typical command sequence is:

puts MIDAS in command mode

H address of module (B - M)

1

0

number of steps desired

2

3

: start stepping channel 1 in the forward direction.

It is possible to wait on the module by inserting an * at the end of the command string while under remote control.

NOTE: Panic Feature - *To stop the clock output or correct an error one need only address some other module and then readdress this module. This halts all operations and clears the module to ready it for another input command string.*

The operation of the module proceeds as described below. Upon receiving one of the direction commands the module activates the DIRection level and starts the clock of the appropriate channel. The clock pulses start at the preset minimum frequency and increase linearly at the rate set by the ramp. At the appropriate time the frequency will ramp down at the same rate to reach the minimum before shutting off.

MANUAL OPERATION

The channel select switch enables one of the three channels to be controlled. Only one channel may be operated at a time.

The FWD/REV switch determines the state of the direction output when the run button is depressed.

The STEP/CONT switch selects either a single step or a continuous output in manual operation. In the CONT mode the clock rate will be determined by minimum frequency adjustment.

The RUN button activates the outputs.

CIRCUIT DESCRIPTION

A complete set of schematic diagrams for the modules are shown in Figs. 7 and 8. The printed circuit board layout and parts list is illustrated in Fig. 9 and a timing diagram is given in Fig. 10.

When the module receives an INIT or is readdressed, U5 issues a RESET command which clears the counters U31-U35 to zero and resets clock enable flip-flop U14 and U15. All the other commands are decoded by U2, U6, and U7 from ASCII characters input from the command bus. Any number "0-9" decoded from the bus creates a LOAD pulse at U3 pin 4. This pulse fires a 20 ns monostable (U36) which parallel loads counter U21. Because of the propagation delay between the parallel input and output of the counter chips, successive load pulses shift the data to the next counter in the string (U21-U25).

When a forward or reverse command is decoded, the appropriate direction flip-flop for the specific channel is set-up; a clock enable flip-flop is set (U14A or U14B or U15A), and a GO pulse is created at U20 pin 8. This GO sets both the RUN flip-flop (U39A) and the RAMP CONTROL flip-flop (U39B). A high signal on the RAMP CONTROL line starts the RAMP UP period.

The output of the RUN flip-flop forces a MODB and sets up U38B for synchronization with the leading edge of the first full clock pulse from the CLK1 line. U38B then gates CLK2 to the clock output section. CLK2 begins to count U21-U25 down and U31-U35 up until a LEVEL DETECT signal is generated. This signal inhibits U31-U35 from further counting and denotes the end of the RAMP UP period.

When U40 pin 13 goes high, the count in U21-U25 is less than or equal to the count in U31-U35; and the RAMP CONTROL flip-flop (U39B) is clocked low which starts the ramp down period. During this period U21-U25 are still counting toward zero. When a zero count is attained, a borrow is propagated from U25 which resets the RUN flip-flop and shuts off CLK2.

The ramp generator and consequently the frequency of the CLK1 line is controlled by the level of the RAMP CONTROL line. The comparator U41 senses the state of the line and controls the current generator U42. A high (low) level at the input of U41 will cause U42 to charge (discharge) C21 at a rate controlled by R26. When the voltage on C21 reaches 6.8 volts it is clamped by D4. At this time a LEVEL DETECT signal is generated by U44. The voltage on C21 is buffered by U43, scaled by R32, and level shifted by U45. This signal then drives the VCO (U46) whose minimum frequency is set by R42.

The clock output section contains logic for the manual or automatic control of the clock and direction outputs. Multiplexer U13 normally outputs the sense of the FWD/REV flip-flops, and multiplexer U12 outputs the state of the channel select flip-flops (U14A, U14B, U15A).

Whenever a CLK2 pulse is received, monostable U11 fires. This strobes the enable line of multiplexer U12 which sends a clock pulse (width determined by U11) out the clock line whose channel select flip-flop is set. The normal sense of these clock lines is controlled by the EXOR gates (U16B, U16C, U16D).

Whenever the front panel RUN button is depressed, U19A and U19B are reset and when it is released U19B is set. The output of U19B controls multiplexers U12 and U13. These multiplexers direct the sense of the FWD/REV switch out to the DIRECTION connectors. They also direct the sense of the channel select switch out to the clock connectors and CLK1 to the clock control circuitry. The first CLK1 pulse fires monostable U11 which pulses the enable line of multiplexer U12. The multiplexer, in turn, pulses the selected clock line and clocks up U19A. If the STEP/CONT switch is in STEP position, U19A immediately resets itself and U19B. If this switch is in the continuous position, U19A and U19B are not reset and successive clock pulses are permitted to be sent out the selected clock line until the RUN switch is released. Releasing the RUN switch resets U19A and U19B and stops the clock pulse.

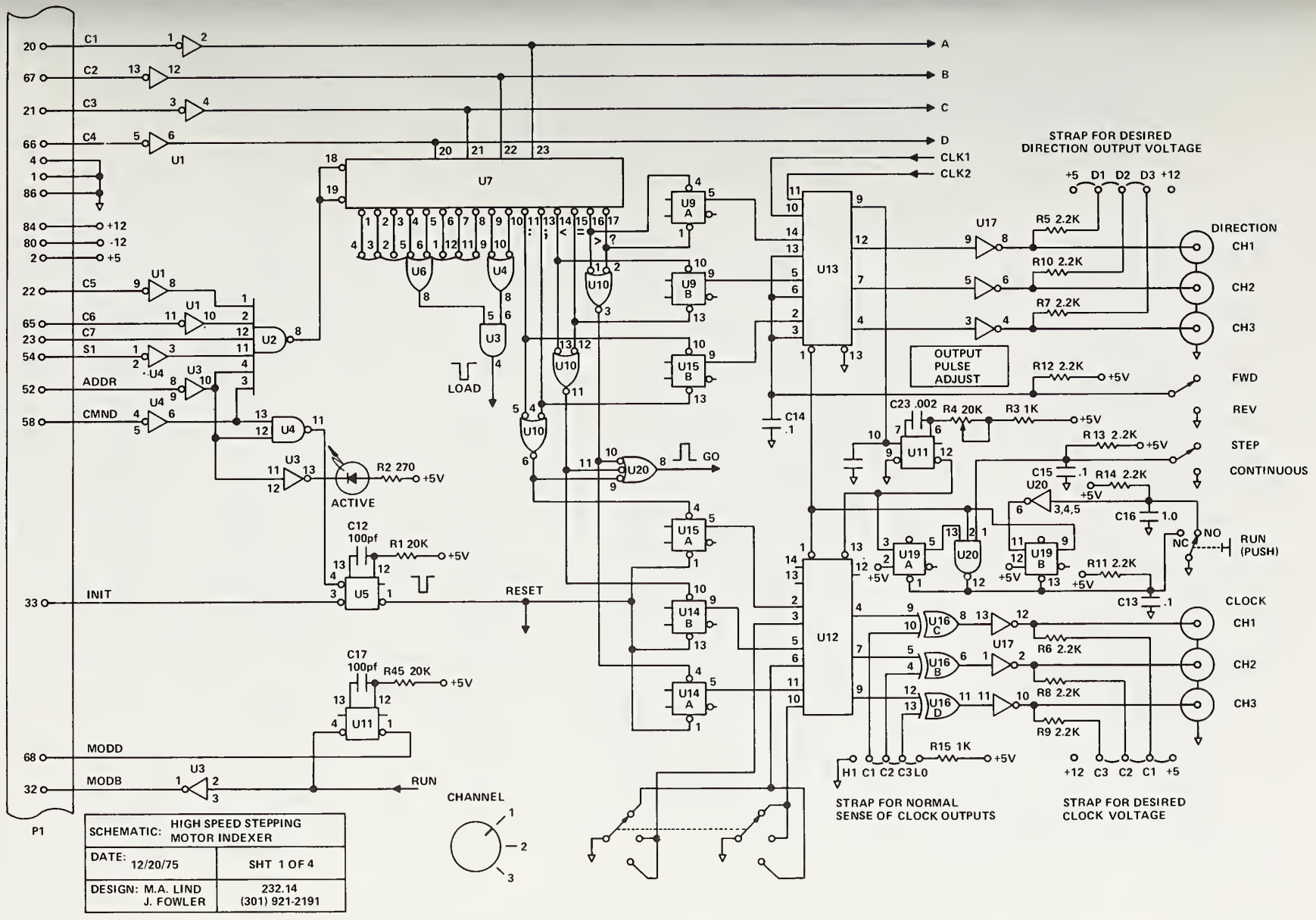


Fig. 7: Schematic diagram for high speed stepping motor indexer: Sheet 1

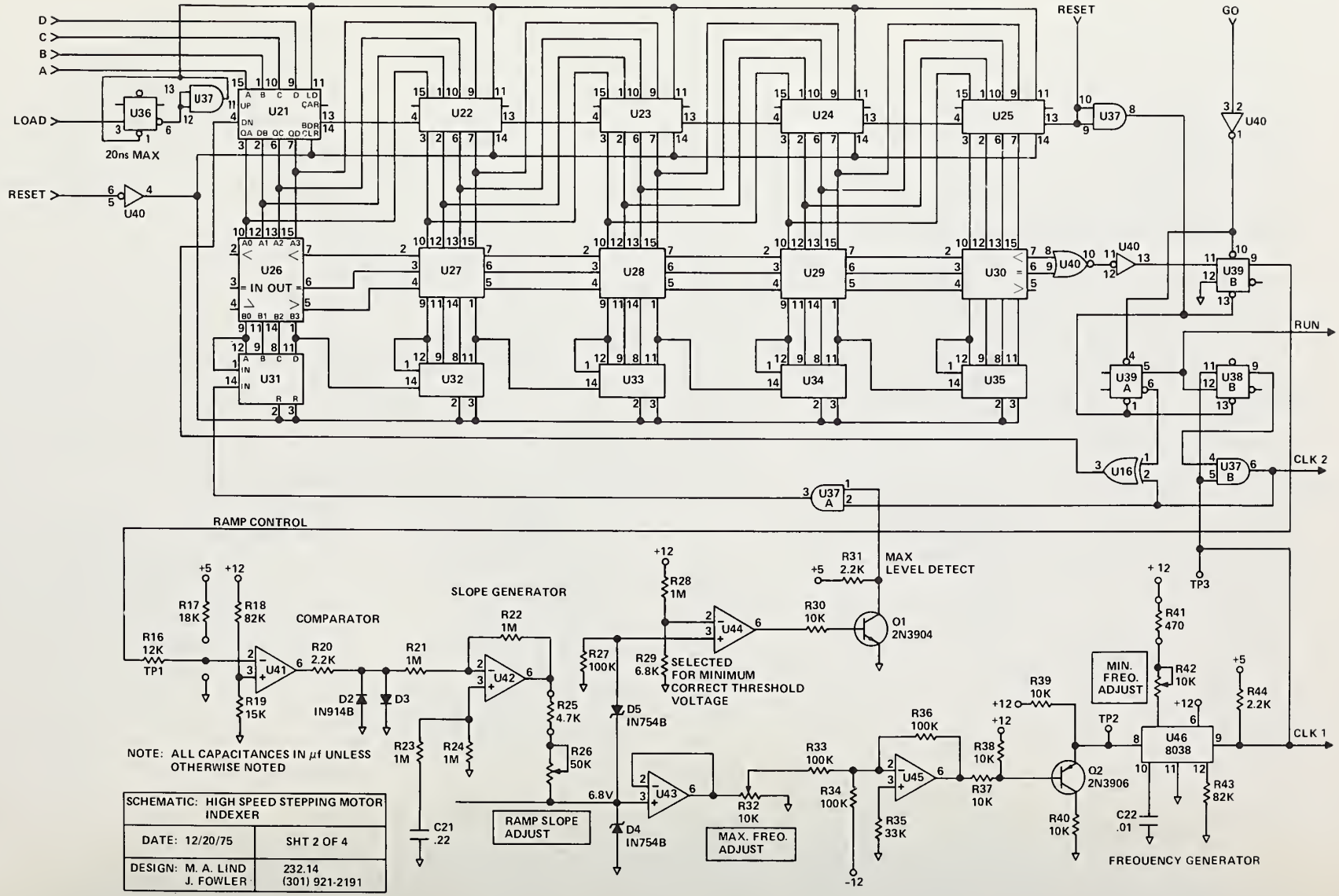


Fig. 8: Schematic diagram for high speed stepping motor indexer: Sheet 2

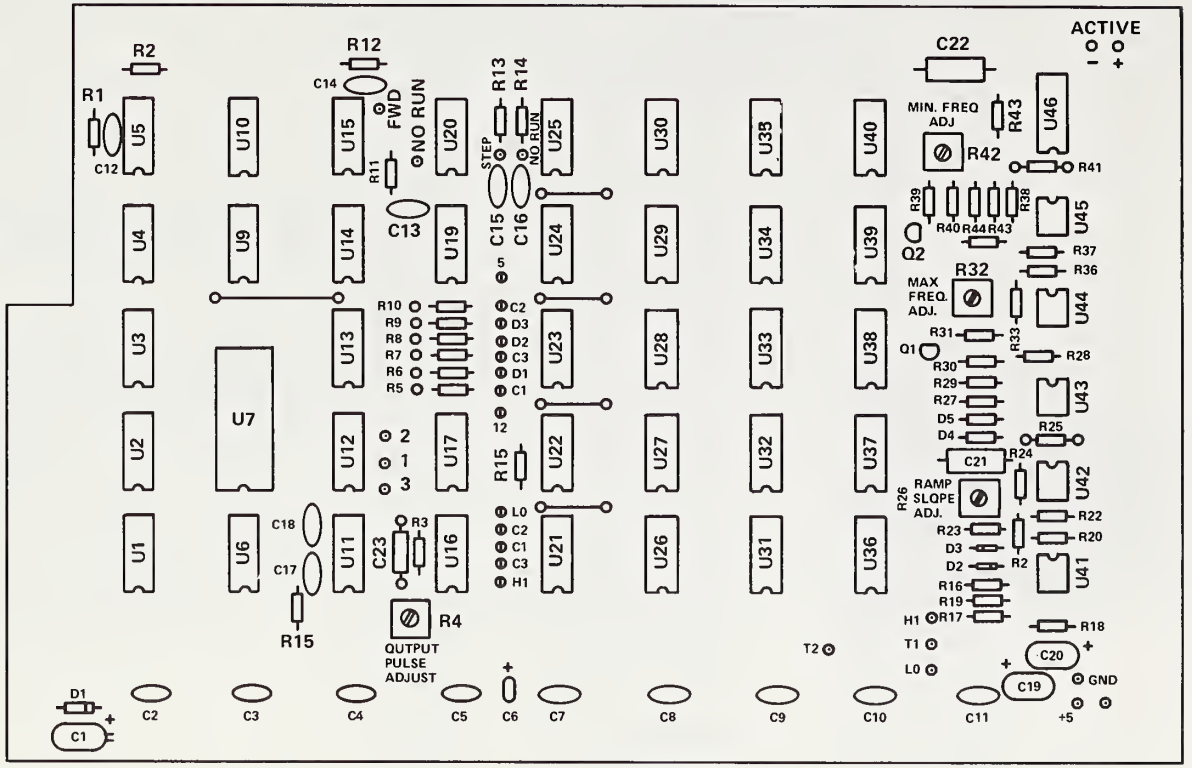
PASSIVE COMPONENTS:

C1	100μf 10V TANT.
C2-C5	
C7-C11	.01μf CER. DISK
C19, C20	10μf, 20V TANT
C6, C18, C16,	1μf, 10V TANT
C12, C17	100pf SILVER MICA
C13-C15	0.1 μf CER. DISK
C21	1μf ELEC.
C22	.01μf MILAR
C23	.002μf MILAR
R1, R45	20K
R2	270Ω
R3, R15	1K
R4	20K CERMET TRIM
R5-R14, R20, R31, R44	2.2K
R16	12K
R17	18K
R18, R43	82K
R19	15K
R21-24, R28	IM
R25	4.7K
R26	50K CERMET TRIM
R27, R36, R33, R34	100K
R29	6.8K SELECTED
R30, R32, R37-R40	10K
R42	10K CERMET TRIM
R41	470Ω

ALL RESISTORS 1/4W TIN OXIDE

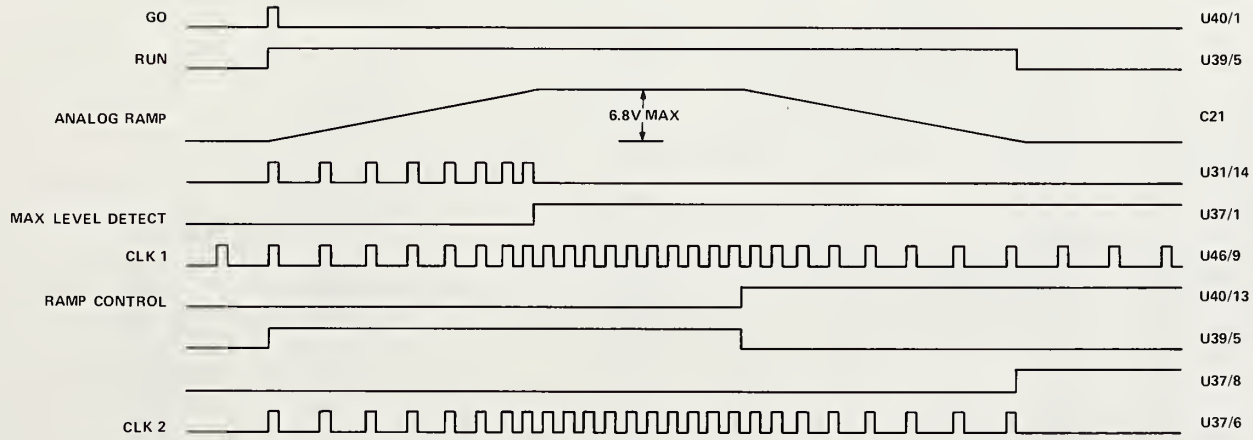
ACTIVE COMPONENTS:

U1	7404	U13	74157	U25	74192	U37	7408	D1	IN4001
2	7430	14	7474	26	7485	38	7474	D2, D3	IN914B
3	7402	15	7474	27	7485	39	7474	D4, D5	IN754
4	7400	16	7486	28	7485	40	7402	Q1	2N3904
5	74121	17	7406	29	7485	41	741	Q2	2N3906
6	7430	18	—	30	7485	42	741		
7	74154	19	7474	31	7490	43	741		
8	—	20	7410	32	7490	44	741		
9	7474	21	74192	33	7490	45	741		
10	7408	22	74192	34	7490	46	INTERSIL 8038		
11	74123	23	74192	35	7490				
12	74157	24	74192	36	74121				



LAYOUT: HIGH SPEED STEPPING MOTOR INDEXER	
DATE: 12/20/75	SHT 3 OF 4
DESIGN: M. A. LIND J. FOWLER	232.14 (301) 921-2191

Fig. 9: Layout and parts list for high speed stepping motor indexer.



MISC. NOTES

1. AFTER THE MODULE IS ADDRESSED, ALL F-F'S AND COUNTERS ARE RESET. THE DOWN COUNTERS (U21-U25) ARE LOADED AND A GO IS ISSUED.
2. THE UP COUNTERS (U31-U35) RECORD THE NUMBER OF CLOCK PULSES DURING THE RAMP UP.
3. WHEN U40/3 GOES HIGH THE TOTAL NUMBER OF COUNTS IN THE DOWN COUNTERS IS LESS THAN OR EQUAL TO THE TOTAL IN THE UP COUNTERS.
4. ALL OUTPUT PARAMETERS (PULSE LENGTH, RAMP RATE, MAXIMUM FREQUENCY, AND MINIMUM FREQUENCY) ARE ADJUSTABLE VIA POTS ON THE P.C. BOARD.
5. OUTPUTS MAY BE MADE EITHER 5V TTL OR 12V CMOS COMPATABLE VIA STRAPPING OPTIONS ON THE BOARD.

MODULE COMMAND	FUNCTION
0-9	ENTER UP TO 5 DIGITS FOR NUMBER OF PULSES TO BE OUTPUT TO CLOCK OUTPUTS
:	CH1 FWD
;	CH1 REV
<	CH2 FWD
=	CH2 REV
>	CH3 FWD
?	CH3 REV

1. SELECTS THE APPROPRIATE OUTPUT CHANNEL AND DIRECTS THE CLOCK PULSES TO IT
2. SETS THE APPROPRIATE LEVEL ON THE DIRECTION OUTPUT AS DETERMINED BY STRAPPING OPTION ON PC BOARD
3. INITIATES THE GO.

TIMING DIAGRAMS:	HIGH SPEED STEPPING MOTOR INDEXER
DATE: 12/20/75	SH 4 OF 4
DESIGN: M. A. LIND J. FOWLER	232.14 (301) 921-2191

Fig. 10: Timing diagrams for high speed stepping motor indexer.

AMPLIFIER CONTROLLER-FILTER-V/F CONVERTER

MODULE DESCRIPTION

This MIDAS compatible module is designed to control a Keithley Model 1800 Programmable Current Amplifier. The amplifier gain is displayed on a front panel readout. There is also included on the board a driver that can be used to activate a relay for remote biasing of the current amplifier, a two pole active filter with an overload indicator, and a bi-polar VCO.

PREOPERATION ADJUSTMENTS

Short the SIGNAL IN connector to ground. Adjust the FILTER TRIM (R28) for a zero reading at the FILTER OUT connector. With the DIRECT/FILTER switch in the DIRECT position adjust the POSITIVE ABS. TRIM (R34) for a zero reading at U26 pin 6, and then adjust the NEGATIVE ABS. TRIM (R33) for a zero reading at U27 pin 6. Next adjust the POLARITY TRIM (R25) so that the POLARITY connector just goes positive, and POSITIVE POLARITY LED just turns on.

Now adjust the VCO TRIM (R32) to give as close to a zero frequency output at the VCO OUT connector as is possible. With 10.000 volts at the SIGNAL IN connector adjust the VCO GAIN (R31) to give a 10.000 kHz signal at the VCO OUT connector.

MIDAS COMMANDS

COMMAND	AMPLIFIER GAIN (A/V)
3	10^{-3}
4	10^{-4}
5	10^{-5}
6	10^{-6}
7	10^{-7}
8	10^{-8}
9	10^{-9}
:	10^{-10}
S	turns on the relay driver
R	turns off the relay driver

CIRCUIT DESCRIPTION

A complete set of schematic diagrams for the module is shown in Figs. 11 and 12. The printed circuit board layout and parts list is illustrated in Fig. 13.

The command lines C1-C7, CMND, ADDR, and S1 are decoded by U1-U5 produce a strobe at U5 pin 13 if any ASCII character "0-15" is detected. The character is then latched in U6 and "5" added to it in U7. The three lower order bits of U7 are complemented to provide the correct code for

the remote programming of the current amplifier. The "R" and the "S" clock the flip-flop U18 low or high respectively. This flip-flop controls Q1 which can be used as a relay driver.

The number stored in the latch U6 is displayed on the front panel. Chips U8-U15 provide for the display multiplexing and the creation of the "-" sign.

The SIGNAL IN from the front panel feeds a bi-polar over voltage detector (U20, U21). A voltage of greater than ±12 volts at the SIGNAL IN cause Q14 to turn on and trigger the monostable U16. The output of the monostable is wire ORed to the level itself to indicate both long and short term overload conditions. U19 then drives the PREFILTER OVERLOAD indicator.

The SIGNAL IN also feeds a two pole adjustable active filter (U23, U24). The output of U24 is fed into a buffer amplifier which drives the FILTER OUT connector.

The input to the precision rectifier (U26, U27) comes either directly from the SIGNAL IN or from the output of the filter via S3. The output of the rectifier drives the high stability VCO (U28). The polarity of the signal is detected by U22 which drives the POSITIVE POLARITY indicator and the POLARITY output.

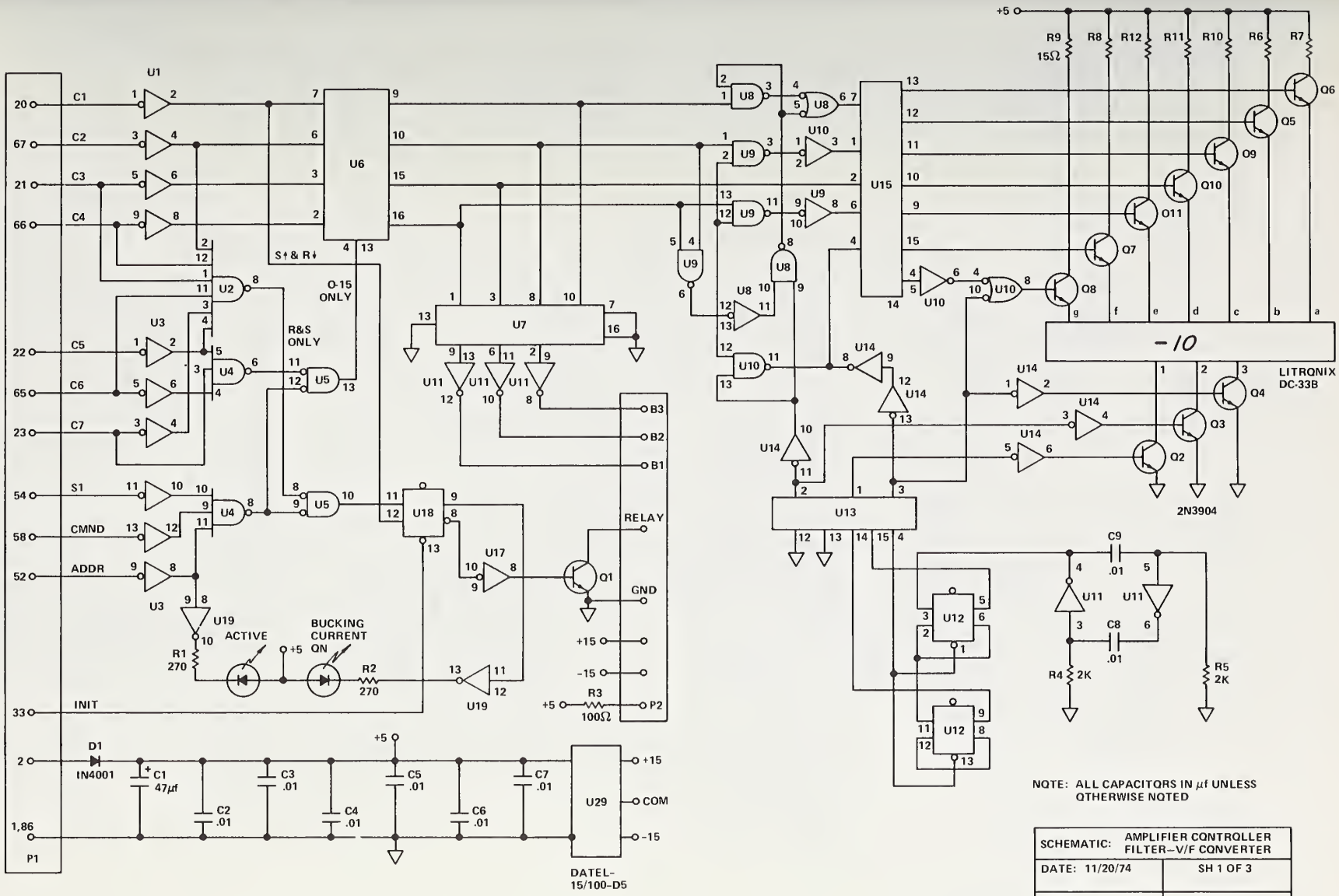


Fig. 11: Schematic diagram for amplifier controller-filter-V/F converter: Sheet 1

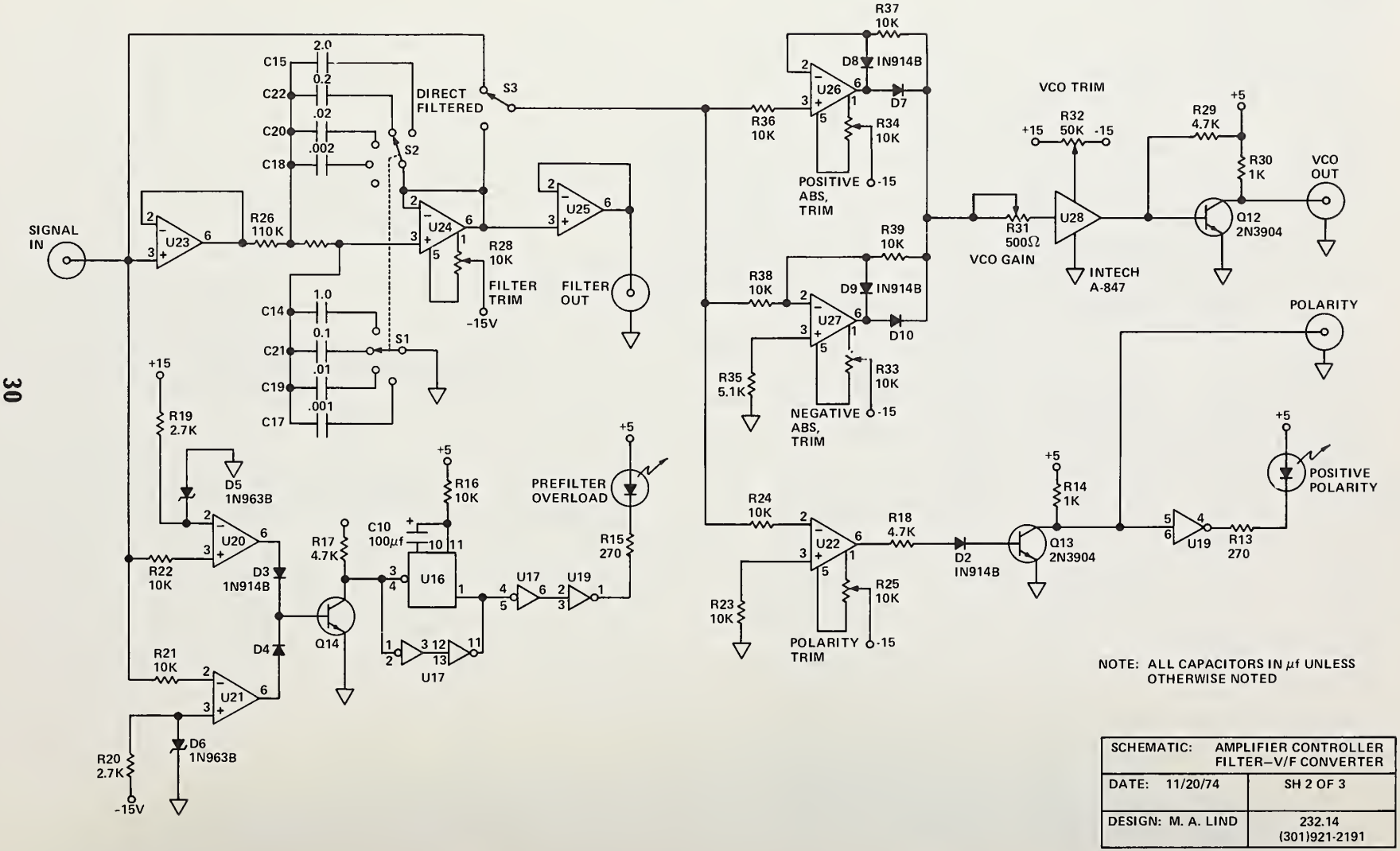


Fig. 12: Schematic diagram for amplifier controller-filter-V/F converter: Sheet 2

ACTIVE COMPONENTS:

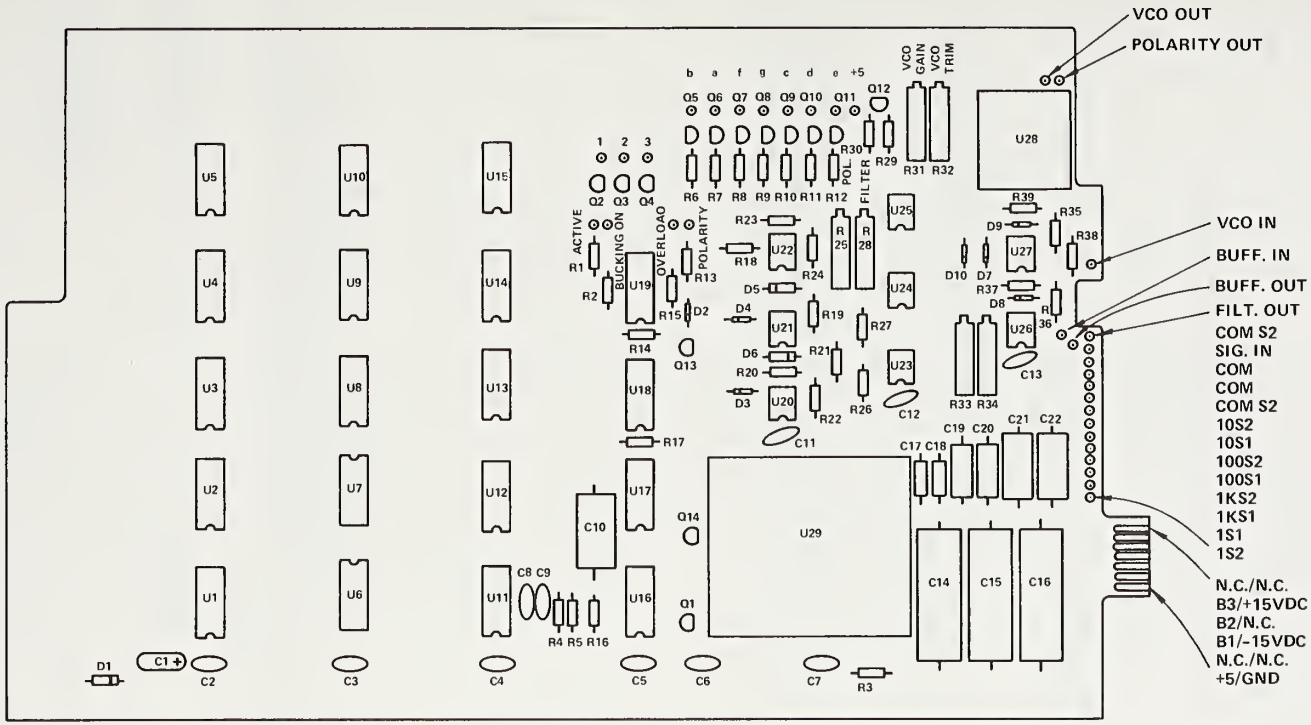
U 1	7404	U11	7404	U21	741
2	7430	12	7474	22	741
3	7404	13	7442	23	741
4	7410	14	7404	24	741
5	7402	15	7448	25	741
6	7475	16	74121	26	741
7	7483	17	7400	27	741
8	7400	18	7474	28	INTECH A-847 V/F
9	7400	19	7401	29	DATEL BPM15/100 D5
10	7400	20	741		

Q1-Q12	2N3904
D1	1N4001
D2-D4	1N914B
D7-D10	
D5, D6	1N963B

PASSIVE COMPONENTS:

C1	47μf TANT
C2-C9, C11-C13	.01μf CER.
C10	100μf ELECTROLITIC
C14-C16	1.0μf MYLAR
C17	.001μf MYLAR
C18	.002μf MYLAR
C19	.01μf MYLAR
C20	.02μf MYLAR
C21	0.1μf MYLAR
C22	0.2μf MYLAR
R1, R2, R13, R15	270Ω
R6-R12	15Ω
R3	100Ω
R4, R5	2K
R14, R30	1K
R16, R21-R24, R36-R39	10K
R17, R18, R29	4.7K
R19, R20	2.7K
R25, R28, R33, R34	10K 15 TURN CERMET
R26, R27	110K
R31	500Ω 15 TURN CERMET
R32	50K 15 TURN CERMET
R35	5.1K

ALL RESISTORS 1/4W TIN OXIDE



LAYOUT: AMPLIFIER CONTROLLER–FILTER–V/F CONVERTER	
DATE: 11/20/74	SH 3 OF 3
DESIGN: M.A. LIND	232.14 (301) 921-2191

Fig. 13: Layout and parts list for amplifier controller-filter-V/F converter.

NBS-114A (REV. 7-73)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBS TN-958	2. Gov't Accession No.	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

FOUR VERSATILE MIDAS COMPATIBLE MODULES

5. Publication Date: November 1977

6. Performing Organization Code

7. AUTHOR(S)

Michael A. Lind and Joel B. Fowler

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

10. Project/Task/Work Unit No.

11. Contract/Grant No.

12. Sponsoring Organization Name and Complete Address *(Street, City, State, ZIP)*

Same as Item 9

13. Type of Report & Period Covered

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

Four versatile MIDAS compatible modules are documented. These modules include a precision digital to analog converter, a programmable up/down counter, a high speed stepping motor indexer, and an amplifier controller-filter-V/F converter.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)* Data acquisition system; MIDAS; MIDAS amplifier controller; MIDAS digital to analog converter; MIDAS modules; MIDAS stepping motor indexer; MIDAS up/down counter.

18. AVAILABILITY

[X] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[X] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Cat. No. C13.46:958

[ ] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151

19. SECURITY CLASS (THIS REPORT): UNCLASSIFIED

21. NO. OF PAGES: 34

20. SECURITY CLASS (THIS PAGE): UNCLASSIFIED

22. Price

USCOMM-DC 29042-P74

NBS TECHNICAL PUBLICATIONS

PERIODICALS

JOURNAL OF RESEARCH—The Journal of Research of the National Bureau of Standards reports NBS research and development in those disciplines of the physical and engineering sciences in which the Bureau is active. These include physics, chemistry, engineering, mathematics, and computer sciences. Papers cover a broad range of subjects, with major emphasis on measurement methodology, and the basic technology underlying standardization. Also included from time to time are survey articles on topics closely related to the Bureau's technical and scientific programs. As a special service to subscribers each issue contains complete citations to all recent NBS publications in NBS and non-NBS media. Issued six times a year. Annual subscription: domestic $17.00; foreign $21.25. Single copy, $3.00 domestic; $3.75 foreign.

Note: The Journal was formerly published in two sections: Section A "Physics and Chemistry" and Section B "Mathematical Sciences."

DIMENSIONS/NBS (formerly Technical News Bulletin)—This monthly magazine is published to inform scientists, engineers, businessmen, industry, teachers, students, and consumers of the latest advances in science and technology, with primary emphasis on the work at NBS. The magazine highlights and reviews such issues as energy research, fire protection, building technology, metric conversion, pollution abatement, health and safety, and consumer product performance. In addition, it reports the results of Bureau programs in measurement standards and techniques, properties of matter and materials, engineering standards and services, instrumentation, and automatic data processing.

Annual subscription: Domestic, $12.50; Foreign $15.65.

NONPERIODICALS

Monographs—Major contributions to the technical literature on various subjects related to the Bureau's scientific and technical activities.

Handbooks—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

Special Publications—Include proceedings of conferences sponsored by NBS, NBS annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

Applied Mathematics Series—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

National Standard Reference Data Series—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a world-wide program coordinated by NBS. Program under authority of National Standard Data Act (Public Law 90-396).

NOTE: At present the principal publication outlet for these data is the Journal of Physical and Chemical Reference Data (JPCRD) published quarterly for NBS by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements available from ACS, 1155 Sixteenth St. N.W., Wash., D.C. 20056.

Building Science Series—Disseminates technical information developed at the Bureau on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

Technical Notes—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NBS under the sponsorship of other government agencies.

Voluntary Product Standards—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The purpose of the standards is to establish nationally recognized requirements for products, and to provide all concerned interests with a basis for common understanding of the characteristics of the products. NBS administers this program as a supplement to the activities of the private sector standardizing organizations.

Consumer Information Series—Practical information, based on NBS research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

Order **above** *NBS publications from: Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.*

Order **following** *NBS publications—NBSIR's and FIPS from the National Technical Information Services, Springfield, Va. 22161.*

Federal Information Processing Standards Publications (FIPS PUB)—Publications in this series collectively constitute the Federal Information Processing Standards Register. Register serves as the official source of information in the Federal Government regarding standards issued by NBS pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

NBS Interagency Reports (NBSIR)—A special series of interim or final reports on work performed by NBS for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Services (Springfield, Va. 22161) in paper copy or microfiche form.

BIBLIOGRAPHIC SUBSCRIPTION SERVICES

The following current-awareness and literature-survey bibliographies are issued periodically by the Bureau:

Cryogenic Data Center Current Awareness Service. A literature survey issued biweekly. Annual subscription: Domestic, $25.00; Foreign, $30.00.

Liquified Natural Gas. A literature survey issued quarterly. Annual subscription: $20.00.

Superconducting Devices and Materials. A literature survey issued quarterly. Annual subscription: $30.00. Send subscription orders and remittances for the preceding bibliographic services to National Bureau of Standards. Cryogenic Data Center (275.02) Boulder, Colorado 80302.

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
Washington, D.C. 20234

OFFICIAL BUSINESS

Penalty for Private Use, $300

POSTAGE AND FEES PAID
U.S. DEPARTMENT OF COMMERCE
COM-215

SPECIAL FOURTH-CLASS RATE
BOOK